I Year II Semester	L	T	P	C
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Code: 17EC201

DIGITAL LOGIC DESIGN

OBJECTIVE:

1. To introduce the basic tools for design with combinational and sequential digital logic and state machines.
2. To learn simple digital circuits in preparation for computer engineering.

UNIT- I: Digital Systems and Binary Numbers

Digital Systems, Binary Numbers, Binary Numbers, Octal and Hexadecimal Numbers, Complements of Numbers, Complements of Numbers, Signed Binary Numbers, addition and subtraction

UNIT -II: Concept of Boolean algebra

Basic Theorems and Properties of Boolean algebra, Boolean Functions, Canonical and Standard Forms, Minterms and Maxterms,

UNIT- III: Gate level Minimization

Map Method, Two-Variable K-Map, Three-Variable K-Map, Four Variable K-Maps. Products of Sum Simplification, Sum of Products Simplification, Don't – Care Conditions, NAND and NOR Implementation, Exclusive-OR Function

UNIT- IV: Combinational Logic

Introduction, Analysis Procedure, Design Procedure, Binary Adder–Subtractor, Decimal Adder, Binary Multiplier, Decoders, Encoders, Multiplexers, HDL Models of Combinational Circuits

UNIT- V: Synchronous Sequential Logic

Introduction to Sequential Circuits, Storage Elements: Latches, Storage Elements: Flip-Flops, Analysis of Clocked **Sequential** Circuits, Mealy and Moore Models of Finite State Machines

UNIT -VI: Registers and Counters

Registers, Shift Registers, Ripple Counters, Synchronous Counters, Ring Counter, Johnson Counter, Ripple Counter

OUTCOMES:

1. A student who successfully fulfills the course requirements will have demonstrated:
2. An ability to define different number systems, binary addition and subtraction, 2'scomplement representation and operations with this representation.
3. An ability to understand the different switching algebra theorems and apply them forlogic functions.
4. An ability to define the Karnaugh map for a few variables and perform an algorithmicreduction of logic functions.

5. An ability to define the other minimization methods for any number of variablesVariable Entered Mapping (VEM) and Quine-MeCluskey (QM) Techniques and performan algorithmic reduction of logic functions.

TEXT BOOKS:

1. Digital Design, 5/e, M.Morris Mano, Michael D Ciletti, PEA.
2. Fundamentals of Logic Design, Charles H. Roth, 5/eCengage.

REFERENCE BOOKS:

1. Digital Logic and Computer Design, M.Morris Mano, PEA.
2. Digital Logic Design, Leach, Malvino, Saha, TMH.
3. Modern Digital Electronics, R.P. Jain, TMH.