II Year II Semester	**L**	**T**	**P**	**C**
Code:20CS4613	**3**	**0**	**0**	**3**

ADVANCED COMPUTER ARCHITECTURE (Honors)

Course Objectives:

The course objectives of Advanced Computer Architecture are to discuss and make student familiar with the

1. Understand the Concept of Pipeline and vector processing
2. Discuss pipelining and superscalar techniques
3. Understand the performance of different memories of Computers.
4. Introduce the advanced processor architectures.
5. Study about scalability and data flow computer architectures.

Course Outcomes:

By the end of the course, the student will:

1. Demonstrate concepts the Concept of Pipeline and vector processing.
2. Discuss Pipelining and Superscalar Techniques.
3. Interpret the performance of different memory techniques like Bus Cache and Shared memory.
4. Gain knowledge of Parallel and Scalable Architectures.
5. Explain Multithreaded and Dataflow Architectures for scalability.

UNIT I

Pipeline and Vector Processing: Parallel processing, pipelining, arithmetic pipeline, instruction pipeline, RISC pipeline, vector processing, array processors.

UNIT II

Pipelining and Superscalar Techniques: Linear Pipeline Processors, Asynchronous and Synchronous models, Clocking and Timing Control, Speedup, Efficiency and Throughput, Pipeline Schedule Optimization.

Instruction Pipeline Design: Instruction, Execution Phases, Mechanisms for Instruction Pipelining, Dynamic Instruction Scheduling, Branch Handling Techniques.

UNIT III

Bus Cache and Shared memory: Introduction, Backplane bus systems, Cache Memory organizations, Shared- Memory Organizations, Sequential and weak consistency models, Pipelining and superscalar techniques, Linear Pipeline Processors, Non-Linear Pipeline Processors, Instruction Pipeline design, Arithmetic pipeline design, super scalar pipeline design.

UNIT IV

Parallel and Scalable Architectures: Introduction, Multiprocessor system interconnects, cache coherence and synchronization mechanism, Three Generations of Multicomputer, Message-passing Mechanisms, Vector Processing Principals, Multi-vector Multiprocessors, Compound Vector processing.

UNIT V

Scalable: Introduction, Multithreaded and Dataflow Architectures, Latency-hiding techniques, Principals of Multithreading, Fine-Grain Multicomputer, Scalable and multithreaded Architectures, Dataflow and hybrid Architectures.

Text Books:

1. Computer System Architecture, Morris M. Mano, 3rd edition, Pearson/Prentice Hall India.
2. Advanced Computer Architecture Second Edition, Kai Hwang, Tata McGraw Hill Publishers.

Reference Books:

1. Computer Architecture, Fourth edition, J. L. Hennessy and D.A. Patterson. ELSEVIER.
2. Advanced Computer Architectures, S.G. Shiva, Special Indian edition, CRC, Taylor & Francis.
3. Computer Organization and Architecture, William Stallings ,8th edition, PHI
4. Introduction to High Performance Computing for Scientists and Engineers, G. Hager and G. Wellein, CRC Press, Taylor & Francis Group.
5. Advanced Computer Architecture, D. Sima, T. Fountain, P. Kacsuk, Pearson education.
6. Computer Architecture, B. Parhami, Oxford Univ. Press.