RAGHU ENGINEERING COLLEGE (Autonomous)

(Approved by AICTE, New Delhi & Permanently Affiliated to JNTUGV, Vizianagaram)
NBA and NAAC 'A+' grade accredited Institute.
Dakamarri, Bheemili Mandal, Visakhapatnam – 531162, A.P.
Phone: 08922-248001 / 221122/9963981111, www.raghuenggcollege.com

INSTITUTE VISION

Envisioning to be a world class technical institution by synergizing quality education with ethical values.

INSTITUTE MISSION

- To encourage training and research in cutting-edge technologies.
- To develop and strengthen strategic links with the industry.
- To kindle the zeal among the students and promote their quest for academic excellence.
- To encourage extra-curricular activities along with good communication skills.

QUALITY POLICY

RAGHU Engineering College underscores ethical values along with innovative teaching through an interactive, activity-based pedagogy; establishes the best of infrastructural facilities, inculcates engineering temper among the students through the use of the latest Information and Communication Technologies, and strives for an efficient, responsive and transparent administration in all areas.

Department of Electronics and Communications Engineering

VISION

To grow into a premier engineering department with excellence in teaching, research, and innovation in the field of electronics and communication engineering at par with the global industrial standards catering to the needs of the stakeholders while keeping up with the advancing technology.

MISSION

- M1: To provide excellence in education, research and public services.
- M2: To provide a creative environment through structured teaching and learning process.
- M3: To impart employability-focused education while imbibing the spirit of entrepreneurship.
- M4: To inculcate self-learning attitude, management skills and professional ethics.

PROGRAMME EDUCTIONAL OBJECTIVES(PEOs)
● PEO 1: **Domain Knowledge: -** To have the knowledge and technical skills required to remain productive. ● PEO 2: **Communication Skills & Employability: -** To apply technical knowledge and skills as electronics and communication engineers to provide practical solutions in industrial and governmental organizations. ● PEO 3: **Life Long Learning & Social Concern: -** To achieve success with awareness of entrepreneurship skills and have the ability for lifelong learning by pursuing professional development to meet the emerging and evolving demands for a successful career.

MAPPING OF MISSION STATEMENTS WITH PEOs

MS/PEO	PEO 1	PEO 2	PEO 3
MS 1	3	2	2
MS 2	3	3	2
MS 3	3	2	3
MS4	2	3	3

1-Slight, **2**- Moderate, **3**- Substantial

PROGRAM OUTCOMES	
Graduates of Electrical and Electronics Engineering Will:	
PO 1	Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO 2	Problem analysis: Identify, formulate, review research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO 3	Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO 4	Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO 5	Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
PO 6	The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO 7	Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO 8	Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO 9	Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO 10	Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO 11	Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO 12	Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES (PSOs)

PSO 1: Understand and apply the fundamental concepts of Basic and Engineering Sciences for appropriate up-skilling in the fast-emerging fields of Signal Processing, Image Processing, Communication, Networking, VLSI, Embedded Systems, Analog and Digital Technologies to meet the futuristic industrial achievements.

PSO 2: Apply latest hardware and software tools to solve complex electronics and communication engineering problems along with analytical skills to derive appropriate solutions in the real time applications across varied business and administrative functions.

Mapping of PEOs with POs and PSOs:

PEO/ POs	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PO-8	PO-9	PO-10	PO-11	PO-12	PSO-1	PSO-2
PEO 1	3	3	3	2	2						1	1	3	1
PEO 2	2	3	3	2			2	2		3			3	3
PEO 3						1	1	1	1	2	1	3	3	1

1-Slight**, 2-** Moderate**, 3-** Substantial

2304103-Digital Circuits Design							
Programme &Branch	**B. Tech & ECE**	**Sem**	**Category**	**L**	**T**	**P**	**Credits**
Prerequisites	**Nil**	**3**	**Professional Core**	**3**	**0**	**0**	**3**

Course Objectives:

1. To understand the properties of Boolean algebra, logic operations, and minimization of Boolean functions.
2. To realize combinational logic circuits design.
3. To study and analyze the various logic circuits with HDLs.
4. To classify and design sequential logic circuits
5. To understand the concepts of FSM and compare various Programmable logic devices.

Preamble:	This course covers the topics related to representation numbers in different radix formats, complements and codes. It also introduces the basic gates and their realization in SOP and POS form. Boolean algebra and various logic gates minimization process is introduced. Design principles of combinational and sequential circuits are explained to make the students thorough in design of these circuits.

Course Contents:

Unit-1	**Boolean algebra, logic operations, and minimization of Boolean functions**	Contact Hours: 9

Number Systems and Codes, Representation of unsigned and signed integers, Floating Point representation of real numbers, Laws of Boolean Algebra, Theorems of Boolean Algebra, Realization of functions using logic gates, Canonical forms of Boolean Functions, Minimization of Functions using Karnaugh Maps.

Unit-2	**Combinational Logic Circuits**	Contact Hours: 9

Combinational circuits, Design with basic logic gates, design procedure, adders, subtractors, 4-bit binary adder/ subtractor circuit, BCD adder, carry look- a-head adder, binary multiplier, magnitude comparator, data selectors, priority encoders, decoders, multiplexers, demultiplexers.

Unit-3	**Hardware Description Language**	Contact Hours: 10

Introduction to Verilog - structural specification of logic circuits, behavioral specification of logic circuits, hierarchical Verilog Code, Verilog for combinational circuits - conditional operator, if-else statement, case statement, for loop using storage elements with CAD tools-using Verilog constructs for storage elements, flip-flop with clear capability, using Verilog constructs for registers and counters.

Unit-4	Sequential Logic Circuits	Contact Hours: 9
Basic architectural distinction between combinational and sequential circuits, Design procedure, latches, flip-flops, truth tables and excitation tables, timing and triggering consideration, conversion of flip-flops, design of counters, ripple counters, synchronous counters, ring counter, Johnson counter, registers, shift registers, universal shift register.		
Unit-5	**Finite State Machines and Programmable Logic Devices**	Contact Hours: 8
Types of FSM, capabilities and limitations of FSM, state assignment, realization of FSM using flip-flops, Mealy to Moore conversion and vice-versa, reduction of state tables using partition technique, Design of sequence detector. Types of PLD's: PROM, PAL, PLA.		
		Total Hours: 45

Text Books:

1	M. Morris Mano, "Digital Design", 3rd Edition, PHI. (Unit I, II, IV & V)
2	Stephen Brown and ZvonkoVranesic, "Fundamentals of Digital Logic with Verilog Design", 3rd Edition, McGraw-Hill (Unit III)
3	T.R. Padmanabhan, B Bala Tripura Sundari, Design Through Verilog HDL, Wiley 2009. (Unit III)

Reference Books:

1	Charles H. Roth, Jr, "Fundamentals of Logic Design", 4th Edition, Jaico Publishers.
2	ZviKohavi and NirajK.Jha, "Switching and Finite Automata Theory, 3rd Edition, Cambridge University Press, 2010.
3	Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", 2nd Edition, Prentice Hall PTR.
4	D.P. Leach, A.P. Malvino, "Digital Principles and Applications", TMH, 7th Edition.

Web References:

1	https://www.youtube.com/watch?v=BqP6sVYlrr0
2	https://www.youtube.com/watch?v=ibQBb5yEDlQ
3	https://www.youtube.com/watch?v=sUutDs7FFeA

COURSE OUTCOMES: Upon completion of the course, students shall have ability to		**BT Mapped** (Highest Level)
CO 1	Understand the properties of Boolean algebra, logic operations, and apply techniques for minimization of Boolean functions.	L2
CO 2	Analyze combinational logic circuits.	L4
CO 3	Understand the basics of HDLs, program structure and basic language elements of Verilog.	L2
CO 4	Design and analyse the synchronous and asynchronous sequential logic circuits.	L5
CO 5	Classify, design and analyse Finite State Machines	L3

Mapping of Cos with POs and PSOs:

COs/ POs	PO -1	PO -2	PO -3	PO -4	PO -5	PO -6	PO -7	PO -8	PO -9	PO -10	PO -11	PO -12	PSO -1	PSO -2
CO 1	3	2	1	-	-	-	-	-	-	-	-	-	2	-
CO 2	2	3	2	-	-	-	-	-	-	-	-	-	3	-
CO 3	2	3	2	-	-	-	-	-	-	-	-	-	3	-
CO 4	2	3	2	-	-	-	-	-	-	-	-	-	3	-
CO 5	2	3	2	1	-	-	-	-	-	-	-	-	3	-
1 – Slight, 2 – Moderate, 3 – Substantial														

ASSESSMENT PATERN - THEORY							
TEST	**Remembering (K1)%**	**Understanding (K2)%**	**Applying (K3)%**	**Analyzing (K4)%**	**Evaluating (K5)%**	**Creating (K6)%**	**Total%**
MID-1	20	40	40				100
MID-2	10	20	40	30			100
SEE	10	10	60	20			100
*± 3% may be varied							