2304203– Digital Circuits Design Lab							
Programme &Branch	**B. Tech - ECE**	**Sem**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**3**	**Professional Core**	**0**	**0**	**3**	**1.5**

Preamble	Digital Electronics Lab is helpful for the students to acquire the basic knowledge of digital logic levels and its application to construct digital electronics circuits. This course will prepare students to perform the analysis and design of various digital electronic circuits. Designing and implementing digital circuits imparts practical knowledge of working with electronics circuits in students. The innovations and ideas bud from a mind that has hands-on experience of hardware integration. This laboratory also helps students develop the real time problem skills which are an important take-away point of troubleshooting the designed circuits.

List of Experiments

1	Design a simple combinational circuit with four variables to obtain minimal SOP expression and verify the truth table using the Digital Trainer Kit.
2	Design a Code converter using Binary to Gray and Gray to Binary codes using Logic gates.
3	Design a full adder circuit and verify its function table.
4	Design Four variable logic function verification using 8×1multiplexer IC-74X151.
5	Draw the circuit diagram of a one-bit comparator using basic gates and test the output.
6	Design D Flip-Flops & JK Flip-Flop and verify output.
7	Modelling different types of gates: (a) 2-input NAND (b) 2-input OR gate (c) 2-input NOR gate (d) NOT gate (e) 2-input XOR gate (f) 2-input XNOR gate using Verilog HDL.
8	Modelling (a) 3 to 8 Decoder using 2 to 4 decoder b. 4 to 2 Encoder using Verilog HDL.
9	Modelling 4:1 Multiplexer with 2:1 multiplexer using Verilog HDL.
10	Modelling a 4-bit parallel adder/Subtractor using Verilog HDL.
11	Design SR, JK, D and T flipflops using Verilog HDL.
12	Design shift register using Verilog HDL.
13	Design (a) 4-bit asynchronous counter (b) BCD synchronous counter using Verilog HDL.

Total: 30hrs

References/Manuals/Software: Xilinx vivado/ any HDL simulators	
1	**Text Book:** Stephen Brown and ZvonkoVranesic, "Fundamentals of Digital Logic with Verilog Design", 3rd Edition, McGraw-Hill
2	**Laboratory Manual:**
3	**Virtual Labs link:**

COURSE OUTCOMES: On completion of the course, the student will be able to		**BT Mapped** (Highest Level)
CO 1	Construct basic logic gates, design and verify combinational logic circuits	L3
CO 2	Construct and implement higher level combinational logic circuits	L3
CO 3	Design sequential logic circuits and verify their functionality.	L4
CO 4	Understand Verilog hardware description, language (HDL).	L2
CO 5	Design and analyze digital circuits using Verilog HDL.	L4

Mapping of COs with POs and PSOs:

COs/ POs	PO -1	PO -2	PO -3	PO -4	PO -5	PO -6	PO -7	PO -8	PO -9	PO -10	PO -11	PO -12	PSO -1	PSO -2
CO 1	3	2	2	-	-	-	-	-	-	-	-	-	2	-
CO 2	3	3	2	-	-	-	-	-	-	-	-	-	3	-
CO 3	3	2	2	-	-	-	-	-	-	-	-	-	3	-
CO 4	3	1	2	-	-	-	-	-	-	-	-	-	3	-
CO 5	3	2	2	1	-	-	-	-	-	-	-	-	3	2
1 – Slight, 2 – Moderate, 3 – Substantial														