RAGHU ENGINEERING COLLEGE (Autonomous)

(Approved by AICTE, New Delhi &Permanently Affiliated to JNTUK, Kakinada)
NBA and NAAC 'A' grade accredited Institute.
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III Year–II Semester

L	T	P	C
3	0	0	3

20EC6453: SIGNAL PROCESSING

Course Objectives:

- To analyze the Discrete-time signals and systems in time and frequency domains.
- To define and use Discrete Fourier Transforms (DFTs).
- To learn the FIR and IIR Filter design procedures.
- To know the need of Multirate Processing.
- To learn the concepts of DSP Processors.

UNIT I

INTRODUCTION: Introduction to Digital Signal Processing: Discrete time signals & sequences, Classification of discrete-time systems, stability and causality of LTI systems, Discrete-time Fourier Transform (DTFT), Frequency domain representation of discrete time signals and systems. Review of Z-transforms.

UNIT II

DISCRETE FOURIER SERIES & FOURIER TRANSFORMS: Properties of discrete Fourier series, Discrete Fourier transforms: Properties of DFT, Computation of DFT, Fast Fourier transforms (FFT) - Radix-2 decimation in time and decimation in frequency FFT Algorithms, Inverse FFT.

UNIT III

Design of IIR and FIR Digital Filters and Realizations: Analog filter approximations – Butter worth and Chebyshev, Design of IIR Digital filters from analog filters, Characteristics of FIR Digital Filters, frequency response, Design of FIR Digital Filters using Window Techniques, Frequency Sampling technique, Comparison of IIR & FIR filters, Basic structures of IIR systems, Basic structures of FIR systems.

UNIT IV

MULTIRATE DIGITAL SIGNAL PROCESSING: Introduction, Decimation, interpolation, sampling rate conversion, Sub-band Coding of Speech Signals, Basics of Digital Filter Banks.

UNIT V

INTRODUCTION TO DSP PROCESSORS: Introduction to programmable DSPs: Multiplier and Multiplier Accumulator (MAC), Architectures, Pipelining, Special addressing modes, On-Chip Peripherals.

Architecture of TMS 320C5X: Introduction, Bus Structure, Central Arithmetic Logic Unit, Parallel Logic Unit, Memory mapped registers, on- chip registers, On-chip peripherals.

Course Outcomes:

A student who successfully fulfils this course requirement will be able to:

S. No	Course Outcome	BTL
1.	Analyze discrete time signals and systems in time and frequency domain.	L3
2.	Apply FFT algorithm to find DFT of a given signal.	L3
3.	Design a Digital IIR & FIR filter from the given specifications and realize the corresponding IIR & FIR structures from the designed digital filter.	L3
4.	Understand the concept of Multirate signal processing and filter banks.	L2
5.	Understand the key architectural features of DSP Processors.	L2

Correlation of Cos with POs & PSOs:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO 1	3	3	2	-	-	-	-	-	-	-	-	-	3	-
CO 2	3	3	2	-	-	-	-	-	-	-	-	-	3	-
CO 3	3	3	3	-	-	-	-	-	-	-	-	-	3	-
CO 4	2	2	1	-	-	-	-	-	-	-	-	-	2	-
CO 5	1	-	-	-	-	-	-	-	-	-	-	-	-	-

Text Books:

1. Digital Signal Processing, Principles, Algorithms, and Applications: John G. Proakis, Dimitris G.Manolakis, Pearson Education / PHI, 2007.
2. Digital Signal Processors – Architecture, Programming and Applications, B.Venkataramani, M.Bhaskar, TATA McGraw Hill, 2002.

Reference Books:

1. Digital Signal Processing: Andreas Antoniou, TATA McGraw Hill , 2006.
2. Digital Signal Processing: MH Hayes, Schaum's Outlines, TATA McGraw Hill, 2007.
3. DSP Primer - C. Britton Rorabaugh, Tata McGraw Hill, 2005.
4. Digital Signal Processing – Alan V. Oppenheim, Ronald W. Schafer, PHI Ed., 2006.