IV B. Tech – I Semester

(20EC7042) ADVANCED VLSI
(Honors)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
30	70	100	3	1	0	4

Pre-Requisites: VLSI Design

Course Objectives:

- To learn the characteristics of MOS Circuits
- To understand the delay and power calculations of MOS transistors
- To understand the VLSI interconnects and process variation of MOS devices
- To realize the combinational and sequential logic circuits of IC design
- To realize the array subsystem of memories and arithmetic designs

UNIT–I: MOS Transistor Theory:
Introduction, Long Channel I-V Characteristics, C-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics.

UNIT–II: Delay and Power:
Delay: Introduction, RC delay model, Linear Delay Model, Logical Effort of Paths.
Power: Introduction, Dynamic and Static Power consumption, Energy- Delay Optimizations.

UNIT–III: Interconnects and Robustness:
Interconnects: Interconnect Modelling, Interconnect Impact, Interconnect Engineering, Logical Efforts with Wires.
Robustness: Variability, Reliability, Scaling, Statistical Analysis of Variability, Variation Tolerant Design.

UNIT–IV: Combinational & Sequential Circuit Design
Circuit Families, SOI circuit Design, Sub-threshold Circuit Design, Sequencing Static Circuits, Circuit Design of Latches and Flip Flops.

UNIT–V: Datapath and Array Subsystem Design
Addition/Subtraction, one/zero Detector, Comparators, Counters, Code converters, Shifters, Multiplication, SRAM, DRAM, ROM, Serial Access Memories.

Course Outcomes:

After successful completion of the course, the students will be able to:

S.No	Course Outcome	BTL
1	Understand the operation of MOS transistor	L2
2	Analyse and estimate delay and power components in a VLSI Circuit	L5
3	Understand the novel solutions on future VLSI Interconnects and robustness	L2
4	Realize and design of combinational and sequential logic circuits using minimization techniques	L5
5	Design of Adders, Multipliers and memories etc	L5

Correlation of COs with POs& PSOs:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	1	-	-	-	-	-	-	-	-	-	2	-
CO2	2	3	2	-	-	-	-	-	-	-	-	-	3	-
CO3	2	3	2	-	-	-	-	-	-	-	-	-	3	-
CO4	2	3	2	-	-	-	-	-	-	-	-	-	3	-
CO5	2	3	2	1	-	-	-	-	-	-	-	-	3	-

Text Books:

1. Weste and Eshraghian, "Principles of CMOS VLSI Design", Pearson Education, 1999.
2. Wayne Wolf, "Modern VLSI Design" Pearson Education.
3. John. P. Uyemura, John Wiley, "Introduction to VLSI Circuits and Systems",2003.

Reference Books:

1. Kamran Eshraghian, Eshraghian Dougles and A. Pucknell," Essentials of VLSI circuits and systems", PHI, 2005 Edition.
2. John P. Uyemura, "Chip Design for Submicron VLSI: CMOS Layout & Simulation",Thomson Learning.
3. John M. Rabaey, "Digital Integrated Circuits" PHI, EEE, 1997.