IV B.Tech – I Semester

(20EC7326) COMPUTER ARCHITECTURE & ORGANIZATION
(Program Elective-V)

Int. Marks	Ext. Marks	Total Marks		L	T	P	C
30	70	100		3	0	0	3

Pre-Requisites: Digital Electronics, Microprocessors and Microcontrollers.

Course Objectives:
- Discuss the basic concepts and structure of computers.
- Understand concepts of register transfer logic and arithmetic operations.
- Explain different types of addressing modes and memory organization.
- Learn the different types of serial communication techniques.
- Summarize the Instruction execution stages.

UNIT I: Digital Computers
Digital Computers: Introduction, Block diagram of Digital Computer, Definition of Computer Organization, Computer Design and Computer Architecture. Register Transfer Language and Micro operations: Register Transfer language, Register Transfer, Bus and memory transfers, Arithmetic Micro operations, logic micro operations, shift micro operations, Arithmetic logic shift unit. Basic Computer Organization and Design: Instruction codes, Computer Registers, Computer instructions, Timing and Control, Instruction cycle, Memory Reference Instructions, Input – Output and Interrupt.

UNIT II: Microprogrammed Control
Control memory, Address sequencing, micro program example, design of control unit. Central Processing Unit: General Register Organization, Instruction Formats, Addressing modes, Data Transfer and Manipulation, Program Control.

UNIT III: Data Representation
Data types, Complements, Fixed Point Representation, Floating Point Representation. Computer Arithmetic: Addition and subtraction, multiplication Algorithms, Division Algorithms, Floating – point Arithmetic operations. Decimal Arithmetic unit, Decimal Arithmetic operations.

UNIT IV: Input-Output Organization
Input-Output Interface, Asynchronous data transfer, Modes of Transfer, Priority Interrupt Direct memory Access. Memory Organization: Memory Hierarchy, Main Memory, Auxiliary memory, Associate Memory, Cache Memory.

UNIT V: Reduced Instruction Set Computer

CISC Characteristics, RISC Characteristics. Pipeline and Vector Processing: Parallel Processing, Pipelining, Arithmetic Pipeline Instruction Pipeline, RISC Pipeline, Vector Processing, Array Processor. Multi Processors: Characteristics of Multiprocessors, Interconnection Structures, Interprocessor arbitration, Interprocessor communication and synchronization, Cache Coherence schemes.

COURSE OUTCOMES:

After successful completion of the course, the students can be able to

S. No	Course Outcome	BTL
1	Understand the basics of instructions sets and their impact on processor design.	L2
2	Design a simple CPU with applying the theory concepts.	L4
3	Manipulate representations of numbers stored in digital computers	L3
4	Exemplify in a better way the I/O and memory organization.	L4
5	Learn the concepts of parallel processing, pipelining and interprocessor communication.	L2

Correlation of COs with POs & PSOs:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	2	-	-	-	-	-	-	-	-	-	3	-
CO2	3	3	2	-	-	-	-	-	-	-	-	-	2	-
CO3	3	2	1	-	-	-	-	-	-	-	-	-	3	-
CO4	2	2	2	-	-	-	-	-	-	-	-	-	2	-
CO5	3	3	1	-	-	-	-	-	-	-	-	-	3	-

Text Books:

1. Computer System Architecture – M. Morris Mano, Third Edition, Pearson/PHI.
2. Carl Hamacher, Zvonko Vranesic, Safwat Zaky Computer Organization, McGraw-Hill, Fifth Edition, Reprint 2012.
3. John P. Hayes, Computer Architecture and Organization, Tata McGraw Hill, Third Edition, 1998. Reference books.
4. William Stallings, Computer Organization and Architecture-Designing for Performance, Pearson Education, Seventh edition, 2006.

Reference Books:

1. Computer Organization and Architecture – William Stallings Sixth Edition, Pearson/PHI.
2. Structured Computer Organization – Andrew S. Tanenbaum, 4th Edition, PHI/Pearson.
3. Donald e Givone, "Digital Principles and Design", TMH.