IV B.Tech – I Semester

(20EC7413) BASICS OF VLSI DESIGN
(Open Elective-IV)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
30	70	100	3	0	0	3

Pre-Requisites: VLSI Design

Course Objectives:

- To understand MOS device characteristics and to implement simple gates using CMOS logic style with delay and power constraints
- To understand the CMOS fabrication process styles including layout design rules
- To design combinational circuits using different logic styles
- To design sequential circuits using different logic styles
- To use modern EDA tools to simulate and synthesize VLSI circuits

UNIT I: MOS Transistor Theory &CMOS Logic
I-V Characteristics, C-V Characteristics, Non ideal I-V effects of MOS Transistors, Basic gates, DC transfer Characteristics of CMOS inverter, Circuit characterization and performance estimation: Delay estimation, Logical effort and Transistor Sizing. Power Dissipation: Static & Dynamic Power Dissipation.

UNIT II: CMOS Fabrication and Layout
CMOS Process Technology N-well, P-well process, Stick diagram for Boolean functions using Euler Theorem, Layout Design Rule, and generation.

UNIT III: CMOS Combinational Circuit Design
Static CMOS, Ratioed Logic, Cascode voltage Switch Logic, Dynamic circuits, Pass Transistor Circuits, Transmission gate circuits.

UNIT IV: CMOS Sequential Circuit Design
Conventional CMOS Latches and Flip Flops, Pulsed Latches, Resettable and Enabled Latches and Flip Flops.

UNIT V: Sub System Design
Single bit Adder, Carry look ahead adder, Carry propagate Adder, Magnitude Comparator, Barrel Shifter, Signed and unsigned multiplier.

Course Outcomes:

After successful completion of the course, the students can be able to

S. No	Course Outcome	BTL
1	Clear understanding of fundamental concepts of MOS transistors	L2
2	Understand fabrication processes and their impact on the circuit performance	L2
3	Able to design and validate combinational circuits using different logic styles.	L6
4	Able to design and validate sequential circuits using different logic styles.	L6
5	Able to design VLSI circuits at sub-system abstraction level	L6

Correlation of COs with POs & PSOs:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	2	-	-	-	-	-	-	-	-	-	2	3
CO2	2	3	2	-	-	-	-	-	-	-	-	-	2	2
CO3	3	2	2	-	-	-	-	-	-	-	-	-	3	3
CO4	2	2	2	-	-	-	-	-	-	-	-	-	3	3
CO5	3	3	1	-	-	-	-	-	-	-	-	-	3	3

Text Books:

1. Neil H.Weste, Harris, A. Banerjee, CMOS VLSI Design, A circuits and System Perspective, 2014, Fourth Edition, Pearson Education, Noida, India.

Reference Books:

1. Jan M. Rabaey, Anantha Chadrakasan, BorivojeNikolic, Digital Integrated Circuits: A Design Perspective, 2014, Third Edition, Prentice Hall India, New Jersey, US.
2. Yogesh Chauhan, Darsen Duane Lu, Vanugopalan Sriramkumar, Sourabh Khandelwal, Juan Duarte, NavidPayvadosi, Ai Niknejad, Chenming Hu, FinFETModeling for IC Simulation and Design, 2015, Academic Press, Elsevier.