II Year II Semester	**L**	**T**	**P**	**C**
Code: 20ES4006	**3**	**0**	**0**	**3**

DIGITAL LOGIC DESIGN

Course Objectives:

1. To introduce the basics of binary number system
2. To define Boolean theorems and simplification of Boolean expressions
3. To design and analyze different combinational logic circuits
4. To understand sequential logic circuits and design finite state machines
5. To learn basics of registers and counters

Course Outcomes:

A student who successfully fulfils this course requirement will be able to:

1. Discuss different number systems and binary operations.
2. Simplify logic functions using Boolean theorems and K-maps
3. Design and analyze combinational circuits and PLDs
4. Analyze and synthesize Finite State Machines
5. Construct registers and counters

UNIT–I: Digital Systems and Binary Numbers

Digital Systems, Binary Numbers, Number based Conversions, Octal & Hexadecimal Numbers, Complements – r's complement, (r-1)'s complement, Signed binary Numbers, Arithmetic addition and subtraction, Binary Codes, Binary Storage & Registers, Floating Point Representation.

UNIT–II: Concept of Boolean algebra and Gate Level Minimization

Basic Definitions, Axiomatic Definitions, Basic Theorems & Properties of Boolean algebra, Boolean Functions, Canonical and Standard Forms, Digital logic gates, The Map Method – Two-Variable, Three-Variable, Four-Variable K-Maps. Product of Sums Simplification, Sum of Products Simplification, Don't Care Conditions, NAND and NOR Implementation, Exclusive-OR Function

UNIT–III: Combinational Logic

Introduction, Analysis Procedure, Design Procedure – Code Converters, Binary Adder–Subtractor, Decimal Adder, Binary Multiplier, Magnitude Comparator, Decoders, Encoders, Multiplexers, Boolean Function Implementation using Decoders and Multiplexers, **Programmable Logic Devices:** Read only Memory, Programmable Logic Array, Programmable Array Logic.

UNIT–IV: Sequential Logic

Introduction to Sequential Circuits, Latches, Flip-Flops, Analysis of Clocked Sequential Circuits, Mealy and Moore Models of Finite State Machines, Synthesis of Sequential Circuits, State reduction and State Assignment, Design Procedure.

UNIT–V: Registers and Counters

Registers, Shift Registers, Universal Shift register, Ripple Counters – Binary Ripple counter, BCDripple counter, Synchronous Counters – Binary counter, Up-down Counter, BCD counter. Counters with unused states, Ring Counter, Johnson Counter

Correlation of COs with POs & PSOs:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO 1	1	1	-	-	-	-	-	-	-	-	-	-	1	-	-
CO 2	2	1	-	-	-	-	-	-	-	-	-	-	2	-	-
CO 3	-	2	1	-	-	-	-	-	-	-	-	-	3	-	1
CO 4	-	3	2	-	-	-	-	-	-	-	-	-	2	-	1
CO 5	-	2	2	-	-	-	-	-	-	-	-	-	3	-	1

Text Books:

1. Digital Design – M.Morris Mano, Michael D Ciletti, 5th ed., PEA.
2. Digital Electronics: Principles, Devices & Applications – Anil K. Maini, Wiley.

Reference Books:

1. Digital Logic and Computer Design – M.Morris Mano, PEA.
2. Digital Principles and Applications – Leach, Malvino & Saha, 6th ed., McGraw Hill.
3. Modern Digital Electronics – R.P. Jain, TMH
4. An Engineering approach to Digital Design – William I Fletcher, PHI.