Mr. RAVI TEJESVI VALIVETI

Assistant Professor
Department of Electronics & communication Engineering
Raghu Engineering College, Dakamarri - 531162, Andhrapradesh,INDIA
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Interests: Signal Processing, Image Processing, Bio-Medical Signal Processing, Embedded Systems, VLSI.

Course Taught Previously

UG

- Pulse and Digital Circuits (PDC)
- Digital Logic Design (DLD)
- Random Variables and Stochastic Process (RVSP)
- Analog and Digital Communications (ADC)
- Microwave Engineering (MWE)
- Signals and Systems (SS)
- Electromagnetic waves and Transmission lines (EMWTL)
- Linear and Digital IC Applications (LDIC)
- Biomedical Engineering (BME)
- Electronic Devices and Circuits (EDC)
- Microprocessors and Microcontrollers (MPMC)

Laboratories Handled

- Analog and Digital Communications Lab
- Microprocessor Lab (Dealing with 8086, 8051 Micro Controller)
- Electronic Devices Lab (Designing circuits using BJT, FET & CE CC Amplifiers)
- Linear IC Applications Lab
- Digital Logic Design Lab.
- Semiconductor Diodes and Applications Lab.
- Digital Signal Processing Lab.

Publications
International Journals

1. **M. Harish, G.Ramesh Babu, Ravi Tejesvi Valiveti, G. Visalakshi**, "Diseases Detection Using Image Processing" Mukt Shabd Journal, http://shabdbooks.com/Vol-10-Issue-1-2021/ , 2347-3150
2. **Mr.V.Ravi Tejesvi,Dr.G.V.Sridhar,Dr.A.Vamsidhar**, "Deep Learning Model For Ecg Classification To Identify Cardiovascular Diseases," Journal of Xi'an University of Architecture & Technology, https://www.xajzkjdx.cn/, 2020, ISSN No : 1006-7930.
3. **Mr.V.Ravi Tejesvi,Dr.G.V.Sridhar**, "Feature Selection Using Cuckoo Search For Electrocardiogram Signal In Cardiac Arrhythmia," International Journal of Management, Technology And Engineering, http://www.ijamtes.org/, 2018, ISSN NO : 2249-7455 .
4. **Mullu Siva Tejaswini , V. Ravi Tejesvi**, "Design and Simulation of UART Serial Communication Module", International Journal of VLSI System Design and Communication Systems, Volume-06, Jan-Dec-2018, ISSN 2322-0929.
5. **K. H. Santhoshi Kumari , V. Ravi Tejesvi**, "High Throughput Implementation of 64-Bit MAC Multioperand Adders", International Journal of VLSI System Design and Communication Systems, Volume-06, Jan-Dec-2018, ISSN 2322-0929.
6. **M.Kesab Chandrasen, P.Sateesh Kumar, K.S.Guru Murthy** and **V. Ravi Tejesvi**, "Design of Automatic Number Plate Recognition System Using OCR for Vehicle Identification", International Journal & Magazine of Engineering, Technology, Management and Research, Volume No: 3 (2016), Issue No: 1 (January), ISSN No: 2348-4845.
7. **P.Sateesh Kumar, M.Kesab Chandrasen, V.Suresh** and **V. Ravi Tejesvi**, "FPGA Implementation of Peak Detector, 64 Bit BCD Counter and Reset Automatic Block for Pd Detection System Using VHDL Simulation", International Journal & Magazine of Engineering, Technology, Management and Research, Volume No: 3 (2016), Issue No: 1 (January), ISSN No: 2348-4845.
8. **B.Ravi Kiran, D.lakshmi Narayana, B.Naveen and V. Ravi Tejesvi**, "LPC and Wavelet Techniques for Speech Compression", International Journal & Magazine of Engineering, Technology, Management and Research, Volume No: 3 (2016), Issue No: 1 (January), ISSN No: 2348-4845.
9. **Kasina Madhusudhana Rao, V.Ravi Tejesvi** and G. AnanthaRao, "Verilog Implementation of 32 Point FFT Using Radix-2 Algorithm on FPGA Technology," IOSR Journal of Electronics and Communication Engineering (IOSR-JECE), Volume 9, Issue 1, Ver. II (Jan. 2014), PP 40-43
10. **Bodasingi Vijay Bhaskar, Valiveti Ravi Tejesvi** and Reddi Surya Prakash Rao, "Implementation of Radix-4 Multiplier with a Parallel MAC unit using MBE Algorithm," International Journal of Advanced Research in Computer Engineering & Technology (IJARCET), Volume 1, Issue 5, July 2012, ISSN: 2278 – 1323

Conference Proceedings

1. **P.Sateesh Kumar, D.lakshmi Narayana, V. Ravi Tejesvi and M.Kesab Chandrasen**, "FPGA Based Sigma-Delta Analog To Digital Converter For Power Sensing", International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT) – 2016.

Seminars, Workshops and STTPs

S.NO	Title	Institute	No. of weeks / Days	Duration
1	Artificial Intelligence, Machine Learning and Deep Learning With MATLAB and Simulink	REC(A) in association with CAPRICOT Technologies Pvt. Ltd	3 Days	23rd to 25th November 2022
2	Analog & Digital IC Design using CADENCE Design Flow	REC(A) in association with Entuple Technologies Pvt. Ltd	3 Days	26th to 29th October 2022
3	Machine Intelligence for Computer Vision	Indian Institute of Information Technology, Design and Manufacturing	6 Days	28th February to 5th March 2022
4	Deep Learning and Machine Learning in Biomedical Signal Processing	GNITS, GPREC in association with E&ICT Academy, NIT Warangal	12 Days	23rd August to 3rd September 2021
5	IEEE Authorship and Publication Ethics	Education Society Chapter of IEEE Vizag Bay Section	5 Days	14th to 18th December 2020
6	An Integrative approach to impact Ethics and Moral Values in Engineering Education	Ramachandra College of Engineering	5 Days	02nd to 6th November 2020
7	Research Trends in Modern Electronics and e-Communication	GMRIT (Autonomous)	5 Days	27th to 31st October 2020
8	Deep Learning and its Application to Computer Vision Problems	GIET University	1 Day	15th July 2020
9	ASIC-SOC Design Flow Methodology	REC (Autonomous)	1 Day	13th July 2020
10	OBE-NBA Process	NEC (Autonomous)	5 Days	15th -19th May 2020
11	Faculty Awareness Programme on Outcome Based Education (OBE) and NBA Accreditation	Sinhgad Institute of Technology and Science	1 Day	9th May 2020
12	EMRF	GVP College of Engineering.	Three days	22th -24th January 2016

Additional Responsibility

RESPONSIBILITIES WITHIN THE INSTITUTE:

1. Assistant Controller of Examinations, REC.

Member in:

1. IAENG (International Association of Engineers) (Reg no: 296518)